#13B/1-14-04
U. Jones

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.: 09/765,958
Applicant: Bulent Dervisoglu, Laurence H. Cooke
Assignee: **Cadence Design Systems, Inc.**
Filing Date: January 18, 2001
Title: HIERARCHICAL TEST CIRCUIT STRUCTURE FOR CHIPS WITH MULTIPLE CIRCUIT BLOCKS

Examiner: Matthew C. Dooley
Group Art Unit: 2133
Docket No.: 260/085 US (7010052001)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT

Dear Sir:

In response to the Office action of July 29, 2003, please amend this application as follows:

Amendments to the Specification begin on page 2 of this paper.

Amendments to the Claims are reflected in the listing of claims which begins on page 4 of this paper.

Remarks begin on page 8 of this paper.

This response is accompanied by a petition for a one month extension of time to extend the period to respond to the Office action to November 29,2003, and to charge the appropriate fee under 37 C.F.R. § 1.16 and § 1.17.

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